DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 02/19/2008 has been entered.

Response to Arguments

Applicant's arguments filed 02/19/2008 have been fully considered but they are not persuasive.

As to claims 1, 20 and 39, applicant added new limitations as: "access all the peripheral using the single port". However, in paragraphs 46, Jones discloses, "*CompactFlash reader 42 also connects to a PC over IDE connector 46. The IDE converter chip 40 also controls the IDE interface to the host PC, allowing image files to be transferred to the PC form CompactFlash card 16*". Also, in paragraph 47, Jones discloses "*Other kinds of flash-memory cards can also be* ***read*** *by CompactFlash reader 42*". Therefore, Jones discloses the newly added limitations.

As to claims 11, 31 and 39, applicant added new limitations as: "access (all) to M peripheral concurrently using the single port". Firstly, the claim(s) contains subject matter, "accessing peripheral devices concurrently…", which was not described in the

specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. According to the specification, paragraph 28 discloses that the controller 612 is electrically connected to the single port 610 of the IDE channel 616 and allows the host 602 to access each of the peripheral devices 604, 606, 608 through the single port 610. There is no other evidence to support the above subject matter. Secondly, in paragraphs 91, Jones discloses, "*The IDE converter chip 40 executes various routines to perform handshaking with the flash-memory cards and accept data, either serially or* ***in parallel***". Therefore, Jones discloses the newly added limitations.

Regarding to claim 49, see the rejection in the Office Action for detail.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 11, 30, 39, 49 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claims contains subject matter, "accessing peripheral devices concurrently using the single port", which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. According to the specification, paragraph 28 discloses that the controller 612 is electrically connected to the single port 610 of the IDE channel 616 and

allows the host 602 to access each of the peripheral devices 604, 606, 608 through the single port 610. There is no other evidence to support the above subject matter. Correction/Clarification is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claim 49 and 51 are rejected under 35 U.S.C. 102(e) as being anticipated by Jones et al. (US 20030084221, hereafter Jones).

As to claim 49, Jones discloses a method for accessing a plurality of serial interface peripheral devices from a host (fig. 9, par. 44), the method comprising:

coupling a controller (chip 40) to the host (PC 20) though a single port of a predetermined interconnection means, the predetermined interconnection means being designed for providing the host access to a maximum of N device (par 101, 111; *"one drive per connector"*);

coupling M serial interface peripheral devices to the controller (devices 62, 64, 66, 68, and 70), wherein M is greater than N (*more than 1 or 2 devices*); and

accessing all the M serial interface peripheral devices concurrently using the single port (par. 91).

As to claim 51, all limitations are listed in claim 49, further: directly transferring data stored on a first of the M serial interface peripheral devices to a second of the M serial interface peripheral devices via the controller without buffering the data in the host (par. 92-93).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-6, 9-16, 19-25, 28-35, & 38-44, and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones in view of ATA Packet Interface for CD-ROM (Revision 2.6 proposed, hereafter Spec).

As to Claims 1, Jones discloses an electronic system comprising:

a host; (Fig. 9 pc 20)

a controller electrically coupled to the host (chip 40) through a single port (port 46) of a predetermined interconnection means (IDE interface 46), the predetermined interconnection means being designed for providing the host access to a maximum of N devices (par 101, 111); and

M peripheral devices electrically coupled to the controller; (devices 62, 64, 66, 68, and 70) wherein M is greater than N (*more than 1 device*) and

the controller allows the host to access all the peripheral devices using the single port (par. 46-47, col 6 lns 1-10; *All devices can be read by the reader 42 and allowing files to be transferred to the PC via port 46*), and .

new commands are used to specify a target peripheral device (par. 101; "identify")

Jones does not disclose the host (Fig. 9 CPU 92) modifies predetermined existing fields in packets/commands (*Instead, discloses new commands to identify a target device*). However, standard IDE interface uses ATAPI packet commands as a special protocol to allow devices to attach to regular IDE controllers. According to Spec, An ATAPI packet command contains many predetermined existing fields such as an operation code, LBA, MSB… Each operation code is sent from a host computer to an IDE device as a command to specify the operation to be performed. Spec also discloses the reserved operation codes in ATAPI packet commands that are used for future standardized commands. (pages 15, 87, 92; *The use and interpretation of those operation codes may be specified by future extensions to this or other standards*). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement the teaching of Jones in ATAPI packets of Spec, by using the host computer to modify the predetermined existing fields with new commands to specify the target peripheral device, in order to standardize and to expand IDE ports to

handle multiple devices in ATAPI environment (*see* pages 15, 87, 92; Jones col 11 lns 65-67).

As to Claim 2, Jones and Spec disclose the electronic system of claim 1. Jones further discloses the predetermined interconnection means is an Integrated Drive Electronics (IDE) bus (Jones, IDE interface par. 46) or a Serial AT Attachment (SATA) interface.

As to Claim 3, Jones and Spec disclose the electronic system of claim 1. Spec further discloses an IDE task file (page 17). According to the specification, IDE task file is a set of registers used to issue IDE commands needed for operation. Similar to ATAPI packets, task files also have reserved bits for future commands (page 45 further in fig. 9 of application). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement the teaching of Jones in IDE task files, by using the host computer to modify the predetermined existing fields in IDE task files with new commands to specify the target peripheral device, in order to standardize and to expand IDE ports to handle multiple devices in IDE environment (*see* pages 15, 87, 92; Jones col 11 lns 65-67).

As to Claim 4, Jones and Spec disclose the electronic system of claim 3. Spec further discloses the predetermined fields are control codes are reserved for future use (Spec, page 87). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement the teaching of Jones in control code fields of the Spec, by using the host computer to modify the predetermined existing fields in reserved control codes to specify the target peripheral device, in order to standardize

and to expand IDE ports to handle multiple devices in IDE environment (*see* pages 15, 87, 92; Jones col 11 lns 65-67).

As to Claim 5, all limitations are in the electronic system of claim 1, wherein the M peripheral devices electrically coupled to the controller at least comprise an optical storage device (Jones, CD-ROM par. 119) and a non-volatile storage device (62-68 in fig 9).

As to Claim 6, all limitations are in the electronic system of claim 5, wherein the non-volatile storage device is a flash card access device (Jones fig. 9 devices 62-68 in) or a hard-disk drive.

As to Claim 9, all limitations are in the electronic system of claim 1, wherein the M peripheral devices include a first peripheral device (flash-memory cards 62-68 in Fig. 9) and a second peripheral device (disk 70 in Fig. 9), and the controller (chip 40 in Fig. 9) directly transfers data stored on the first peripheral device to the second peripheral device without buffering the data in the host (Jones par 92 & 93).

As per Claim 10, Jones discloses the electronic system of claim 1, wherein the host determines which peripheral devices are coupled to the controller and builds a set of virtual drives (par. 78, 92; drive letter f: - h:) in an operating system (OS) of the host corresponding the peripheral devices coupled to the controller.

As to claim 11, all same limitations are disclosed in claims 1 and 9 with further: the controller allows the host to access the M peripheral devices concurrently using the single port (par. 91 “accept data either serially or in parallel”).

As per Claims 12-16 and 19, all limitations are disclosed in the electronic system of claim 11, with further limitations in claims 2-6, and 10.

As to claim 20, all same limitations are disclosed in claims 1 in method form.

As per Claims 21-25, and 9-10, all limitations are disclosed in the method of claim 20, with further limitations in claims 2-6, and 9-10.

As to claim 30, all same limitations are disclosed in claims 11 in method form.

As per Claims 31-35 and 38, all limitations are disclosed in the electronic system of claim 11, with further limitations in claims 2-6, and 10.

As to claim 39, all same limitations are disclosed in claims 11 further: a memory for storing the data, wherein the memory is shared by the extra (M-N) devices (fig. 10 RAM 94, par. 100).

As per Claims 40-44, and 47-48, all limitations are disclosed in the system of claim 39, with further limitations in claims 2-6, and 9-10.

As to claim 50, all limitations are listed in claim 49 with further limitations in claim 1. Therefore, the supporting rationale of the rejection to Claim 1 applies equally as well to Claim 50.

Claims 7, 8, 17, 18, 26, 27, 36, 37, and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jones in view of Spec, and in further view of Fuller (US 4809164).

As per Claims 7-8, Jones and Spec disclose the electronic system of claim 1, but do not teach the host schedules packets sent to the M peripheral devices according

to a priority ranking wherein the priority ranking is a dynamic ranking that varies according to operations or speed settings of the peripheral devices. However, in the same field of art, Fuller teaches an electronic system, which comprises a processor and plural peripheral devices. Fuller teaches the concept of the setting priority wherein a higher priority is given to those devices that must unload data quickly and a lower priority is given to slower devices (col 2 lns 35-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement the teachings of Fuller into Jones' system, by scheduling packets sent to the M peripheral devices according to according to operations or speed settings of the peripheral devices, in order to provide an improvement of prioritization with plurality of access devices, to provide load balancing between the host and peripheral devices. (col 1 lns 5-40, col 2 lns 35-51).

As per Claims 17-18, Jones and Spec disclose the electronic system of claim 11, but do not teach the host schedules packets sent to the M peripheral devices according to a priority ranking wherein the priority ranking is a dynamic ranking that varies according to operations or speed settings of the peripheral devices. However, in the same field of art, Fuller teaches an electronic system, which comprises a processor and plural peripheral devices. Fuller teaches the concept of the setting priority wherein a higher priority is given to those devices that must unload data quickly and a lower priority is given to slower devices (col 2 lns 35-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement the teachings of Fuller into Jones' system, by scheduling packets sent to the M peripheral

devices according to according to operations or speed settings of the peripheral devices, in order to provide an improvement of prioritization with plurality of access devices, to provide load balancing between the host and peripheral devices. (col 1 lns 5-40, col 2 lns 35-51).

As per Claims 26-27, Jones and Spec disclose the method of claim 20, but do not teach the host schedules packets sent to the M peripheral devices according to a priority ranking wherein the priority ranking is a dynamic ranking that varies according to operations or speed settings of the peripheral devices. However, in the same field of art, Fuller teaches an electronic system, which comprises a processor and plural peripheral devices. Fuller teaches the concept of the setting priority wherein a higher priority is given to those devices that must unload data quickly and a lower priority is given to slower devices (col 2 lns 35-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement the teachings of Fuller into Jones' system, by scheduling packets sent to the M peripheral devices according to according to operations or speed settings of the peripheral devices, in order to provide an improvement of prioritization with plurality of access devices, to provide load balancing between the host and peripheral devices. (col 1 lns 5-40, col 2 lns 35-51).

As per Claims 36-37, Jones and Spec disclose the method of claim 30, but do not teach the host schedules packets sent to the M peripheral devices according to a priority ranking wherein the priority ranking is a dynamic ranking that varies according to operations or speed settings of the peripheral devices. However, in the same field of art, Fuller teaches an electronic system, which comprises a processor and plural peripheral

devices. Fuller teaches the concept of the setting priority wherein a higher priority is given to those devices that must unload data quickly and a lower priority is given to slower devices (col 2 lns 35-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement the teachings of Fuller into Jones' system, by scheduling packets sent to the M peripheral devices according to according to operations or speed settings of the peripheral devices, in order to provide an improvement of prioritization with plurality of access devices, to provide load balancing between the host and peripheral devices. (col 1 lns 5-40, col 2 lns 35-51).

As per Claims 45-46, Jones and Spec disclose the electronic system of claim 39, but do not teach the host schedules packets sent to the M peripheral devices according to a priority ranking wherein the priority ranking is a dynamic ranking that varies according to operations or speed settings of the peripheral devices. However, in the same field of art, Fuller teaches an electronic system, which comprises a processor and plural peripheral devices. Fuller teaches the concept of the setting priority wherein a higher priority is given to those devices that must unload data quickly and a lower priority is given to slower devices (col 2 lns 35-51). Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to implement the teachings of Fuller into Jones' system, by scheduling packets sent to the M peripheral devices according to according to operations or speed settings of the peripheral devices, in order to provide an improvement of prioritization with plurality of access devices, to provide load balancing between the host and peripheral devices. (col 1 lns 5-40, col 2 lns 35-51).

Examiner's note:

Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner.

In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DEAN PHAN whose telephone number is (571)270-1002. The examiner can normally be reached on Mon - Thu; 9:30AM - 5:00PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tariq Hafiz can be reached on (571) 272 6729. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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